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Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	1	"7236921".pn.	US-PGPUB; USPAT	OR	ON	2008/01/22 09:25
S2	77	("20020052729" "20020116168" "20020156885" "20020156998" "20030056071" "20030149961" "4176258" "4757534" "5127103" "5202687" "5321828" "5325512" "5331571" "5371878" "5493723" "5546562" "5559996" "5572665" "5574892" "5587957" "5590354" "5630052" "5630102" "5663900" "5691898" "5748875" "5752013" "5802290" "5805792" "5889988" "5911059" "5964893" "5978584" "5999725" "0559996" "6009270" "6016554" "6016563" "6034538" "6058263" "6075941" "6094730" "6107826" "6144327" "6161199" "6173419" "6185522" "6202044" "6223144" "6223272" "6289300" "6298320" "6302268" "6347395" "6356862" "6366878" "6374370" "6385742" "6460172" "6466898" "6487700" "6516428" "6564179" "6581191" "6618854" "6718294" "6810442" "6816544" "6829727" "6922821" "6957180" "6967960" "7076420" "7089175" "7099818" "7162410" "7236921").PN.	US-PGPUB; USPAT	OR	ON	2008/01/22 09:25
S3	7	S2 and sleep	US-PGPUB; USPAT	OR	ON	2008/01/22 09:25
S4	6	S3 and clock\$1	US-PGPUB; USPAT	OR	ON	2008/01/22 09:44
S5	13	("20020052729" "20020156998" "20030056071" "20030149961" "4176258" "4757534" "5691898" "5802290" "6016563" "6034538" "6460172" "6816544" "6967960").PN.	US-PGPUB; USPAT	OR	ON	2008/01/22 09:50
S6	1	"4757534".PN.	US-PGPUB; USPAT	OR	ON	2008/01/22 09:51
S7	1	"5357626".PN.	US-PGPUB; USPAT	OR	ON	2008/01/22 10:06
S8	36	703/23,26.ccls. and @pd>"20070829"	US-PGPUB; USPAT	OR	ON	2008/01/22 10:15
S9	0	716/224.ccls. and @pd>"20070829"	US-PGPUB; USPAT	OR	ON	2008/01/22 10:15
S10	9	714/28.ccls. and @pd>"20070829"	US-PGPUB; USPAT	OR	ON	2008/01/22 10:15

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S11	59	cypress adj semiconductor\$.as. and @pd>"20070829"	US-PGPUB; USPAT	OR	ON	2008/01/22 10:17
S12	0	S11 and (sleep and (stall or halt))	US-PGPUB; USPAT	OR	ON	2008/01/22 10:16
S13	3	S11 and sleep	US-PGPUB; USPAT	OR	ON	2008/01/22 10:17
S14	1	S11 and stall	US-PGPUB; USPAT	OR	ON	2008/01/22 10:17
S15	1549	cypress adj semiconductor\$.as.	US-PGPUB; USPAT	OR	ON	2008/01/22 10:17
S16	15	S15 and sleep.clm.	US-PGPUB; USPAT	OR	ON	2008/01/22 10:18
S17	10	S16 and clock\$1.clm.	US-PGPUB; USPAT	OR	ON	2008/01/22 10:18
S18	18	S15 and (sleep.clm. or stall.clm.)	US-PGPUB; USPAT	OR	ON	2008/01/22 10:18
S19	10	S18 and clock\$1.clm.	US-PGPUB; USPAT	OR	ON	2008/01/22 10:21
S20	16	nemecek-craig\$.in.	US-PGPUB; USPAT	OR	ON	2008/01/22 10:27
S21	691	((device adj under adj test) or dut) and @pd>"20070829"	US-PGPUB; USPAT	OR	ON	2008/01/22 10:27
S22	0	S21 and (sleep near (mode or function or operation))	US-PGPUB; USPAT	OR	ON	2008/01/22 10:29
S23	0	S21 and (stall near (mode or function or operation))	US-PGPUB; USPAT	OR	ON	2008/01/22 10:28
S24	0	S21 and (clock near off)	US-PGPUB; USPAT	OR	ON	2008/01/22 10:28
S25	5	S21 and sleep	US-PGPUB; USPAT	OR	ON	2008/01/22 10:28
S26	343	(sleep near (mode or function or operation)) and (clock near off)	US-PGPUB; USPAT	OR	ON	2008/01/22 10:30
S27	2	S26 and ((device adj under adj test) or dut)	US-PGPUB; USPAT	OR	ON	2008/01/22 10:30
S28	5	(stall near (mode or function or operation)) and (clock near off)	US-PGPUB; USPAT	OR	ON	2008/01/22 10:31
S29	2	S27 and ((device adj under adj test) or dut)	US-PGPUB; USPAT	OR	ON	2008/01/22 10:38
S30	0	S28 and emulat\$3	US-PGPUB; USPAT	OR	ON	2008/01/22 10:37
S31	55	((device adj under adj test) or dut) and (clock near off)	US-PGPUB; USPAT	OR	ON	2008/01/22 10:38
S32	5	S31 and (sleep or stall or halt)	US-PGPUB; USPAT	OR	ON	2008/01/22 10:38



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 ... other functional unit is awakened from its **sleep** condition ... In comparison, a Xilinx **FPGA** has 8i7 I/O pads ... interconnect is used in a Xilinx -based **emulator** at some ...

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 R Leatherman, B Ableidinger, N Stollon - Proc. Embedded Systems Conference, April, 2003 - [fs2.com](#)
 ... is seen in early (pre-silicon) debug (ie hardware **emulation** or in **FPGA** devices)
 with a ... by a semaphore synchronization until it is put to **sleep** waiting for ...

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 I Part, II Part - [lina.ee.ntu.edu.tw](#)

 ... most common type, can be solved by Forwarding or **Stall** ... the pipeline, the worst the branch penalty in **clock** cycles ... Until the trap is taken, turn **off** all writes ...

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[\[PDF\] FPGA-Accelerated Simulation Technologies \(FAST\): Fast, Full-System, Cycle-Accurate Simulators](#)

 D Chiou, D Sunwoo, J Kim, NA Patil, W Reinhart, DE ... - [users.ece.utexas.edu](#)
 ... extensive paral- lelism and high **clock** frequencies to ... models to be implemented in a single **FPGA**. ... ignores incorrect path instructions and **stalls** until correct ...

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 JR Andrews - 2004 - [books.google.com](#)

 ... code into a suitable bitstream file for programming the **FPGA**. ... the CPU board for in-circuit **emulation** of ARM ... not active) can be minimized using **sleep** modes and ...

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[\[PDF\] PowerAnalyzer for Pocket Computers - all 2 versions »](#)

 T Austin, T Mudge, U Michigan, D Grunwald, U ... - Online Article, <http://www.eecs.umich.edu/panalyzer/pdfs> ..., 2001 - [eecs.umich.edu](#)

 ... XScale + **FPGA** ... ARM ISA **emulation** support added to SimpleScalar tool set ... eg, branch mispredictions, cache misses, writeback **stalls** ...

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[Temperature aware task scheduling in MPSoCs - all 2 versions »](#)

 AK Coskun, TS Rosing, K Whisnant - Proceedings of the conference on Design, automation and test ..., 2007 - [portal.acm.org](#)

 ... However, **sleep** state of the cores typically consume power much less than the active state, and ... A fast HW/SW **FPGA**-based thermal **emulation** framework for ...

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J del Cuvillo, W Zhu, Z Hu, GR Gao - Proceedings of the Workshop on Modeling, Benchmarking and ... - caps1.udel.edu

... groups) operating at a moderate **clock** rate (500MHz). ... instructionbefore it is available, the pipeline will **stall**. ... The **sleep** instruction, the wakeup signal, the ...

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[PDF] [Giano: The Two-Headed System Simulator](#) - all 3 versions »

A Forin, B Neekzad, NL Lynch - research.microsoft.com

... A desirable property of an **FPGA** device is ... of the various processors because bus contention, **stalls** and interrupts ... to context switch with a minimal **sleep**, and (2 ...

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S Lee - 1993 - bwrc.eecs.berkeley.edu

... 9 : Output from **Clock** Generator.....67 ... **Emulation** Kernel Multiple **FPGA**-Based Logic ...

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D Bekker - 2007 - ritdml.rit.edu

... run times on fully functional hybrid-**FPGA** systems built with Xilinx's ... replaces string manipulation functions and standard floating-point **emulation** with hand- ...

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[PDF] [Multimedia Terminal System-on-Chip Design and Simulation - all 5 versions »](#)

I Barbieri, M Bariani, A Scotto, M Raggio - EURASIP Journal on Applied Signal Processing, 2005 - hindawi.com

... of a device multiplexing the media streams, and the **emulation** of the ... cycles entry in Table 1 represents the number of **clock** cycles without **stalls** due to ...

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A Sinha, A Chandrakasan - Power Aware Computing, 2002 - books.google.com

... on the StrongARM uses a software **emulation** to implement it ... is also performed to determine **stalls** and a ... However, reverting to **sleep** mode between duty cycles may ...

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L Levinson - atlas-proj-tgc.web.cern.ch

... simulated events were sent from the Star Switch **Emulator** to the ... In addition to low skew **clock** distribution over the **FPGA**, the digital **clock** managers, DCMs ...

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[PDF] [The First Annual Workshop on Modeling, Benchmarking, and Simulation \(MoBS-1\)](#)

W Madison - arctic.umn.edu

... processor with Hyper-threading (a version of SMT) [5]. The benchmarks were chosen based on their long run-times, which allows a longer start time **off**- sets to ...

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[CITATION] [Harnessing FPGAs for Computer Architecture Education](#) Mark Holland

M Holland, S Hauck, C Ebeling

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[Processor-controller interface for non-lock step operation - all 2 versions »](#)

KS Purcell, AR Ansari - US Patent 7,243,212, 2007 - Google Patents

... 3-75 through 3-96. Xilinx, Inc.; "Virtex-II Platform **FPGA** Handbook"; published Dec. ... Xilinx, Inc.; "Virtex-II Pro Platform **FPGA** Handbook"; published Oct. ...

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T Simunic, L Benini, G De Micheli - Very Large Scale Integration (VLSI) Systems, IEEE ..., 2001 - ieeexplore.ieee.org

... Field programmable gate array (**FPGA**) hardware emu- lators are ... an on-chip cache miss, the processor **stalls** and ex ... might have two idle states: refresh and **sleep**. ...

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[Access to a bank of registers of a device control register interface using a single address -](#)

all 2 versions »

AR Ansari, KS Purcell - US Patent 7,200,723, 2007 - Google Patents

... 3-75 through 3-96. Xilinx, Inc.; "Virtex-II Platform **FPGA** Handbook"; published Dec. ...

33-75. Xilinx, Inc.; "Virtex-II Pro Platform **FPGA** Handbook"; published Oct. ...

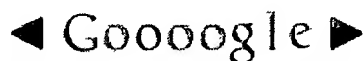
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TC Hiers - 2001 - csg.lcs.mit.edu

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D Kouzis-Loukas - 2006 - doit4me.gr

... Architecture overview of Virtex II Pro **FPGA**... ... a core may take several **clock** cycles to ... creates a trade-off between how ...

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[Processor design based on dataflow concurrency - all 5 versions »](#)

SG Ziavras - Microprocessors and Microsystems, 2003 - Elsevier

... cache and the local memory of the **FPGA** must be ... flow of instructions in CPU pipelines, with reduced **stalls**. ... Therefore, they **sleep** until they are forced into the ...

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P Platform - diva-portal.org

... Some techniques allow reprogrammability and some allows for the **FPGA** to retain their contents on power-off. These are the different techniques available:[20] ...

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[S: USA+ N: Martin Devera+ E: devik@ cdi. cz+ W: http://luxik. cdi. cz/~ devik/qos/+ D: HTB qdisc and ...](#)

NW Muees, BK Concepts - nrc.ca

... changes, but hold **off** net-drivers-2.5 because of a change that needs. +more discussion. +. ... If both this SCSI **emulation** and native ATAPI support are compiled. ...

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A Koch - esa.informatik.tu-darmstadt.de

... instruction would stop the flow (**stall** the pipeline). ... operations per second per MHz **clock** frequency per ... as Field-Programmable Gate Arrays (**FPGA**) was developed ...

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[PDF] [RTSS 2004 Work-In-Progress Proceedings Lisbon, Portugal December 6-8 2004](#)

P Lisbon - cs.utah.edu

... SOFT REAL-TIME PROCESSING IN AN INTEGRATED SYSTEM Caixue Lin and Scott A. Brandt • FAST SYNCHRONIZATION PRIMITIVES FOR HYBRID CPU/**FPGA** MULTITHREADING R. Jidin ...

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J Masel, B Zabarski, I Greenblat - 2003 - freepatentsonline.com

... Telegraph and Telephone CES Circuit **Emulation** Services CLEC ... useful in prototyping future peripherals by **FPGA**-extending existing ... Then for one **clock** it is negated ...

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B Zabarski, M Tarrab, O Norman - 2003 - freepatentsonline.com

... Telegraph and Telephone CES Circuit **Emulation** Services CLEC ... in prototyping future peripherals by **FPGA**-extending existing ... it does not introduce one **clock** delay. ...

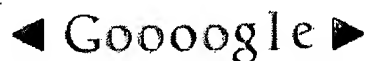
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... Client-Server [2195]. Climbing [2519, 488]. Clinical [1933, 2673, 272, 2151]. Cliques [831]. **Clock** [1225]. Clocked [1243]. Clocks [1475, 1471]. Clones [2061]. ...

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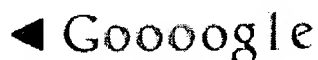
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A De Vivo - udsab.dia.unisa.it

... is sent to the sender to **stall** the transmission ... QNIX design is based on **FPGA** technology, allowing ... driven communication which allows them to **sleep** until messages ...[Related Articles](#) - [View as HTML](#) - [Web Search](#)Result Page: [Previous](#) [1](#) [2](#) [3](#) [4](#)[Google Home](#) - [About Google](#) - [About Google Scholar](#)

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